

## CLAIMS

What is claimed is:

5        1. A non-volatile memory device comprising:  
an array of memory cells arranged in rows and columns;  
a plurality of page buffers connected to the columns, wherein each of the page buffers  
comprises a bias transistor connected between a corresponding column and a corresponding  
sense node, a latch connected to the corresponding sense node, and a precharge transistor  
10      connected between a power supply voltage and the corresponding sense node; and  
a control logic configured to control the page buffers during a read operation, wherein  
the control logic is configured to control the bias and precharge transistors of respective page  
buffers to fix second sense nodes at a predetermined bias voltage during a first sensing period  
when voltages on first sense nodes are being sensed.

15      2. A non-volatile memory device according to claim 1, wherein the control logic  
is configured to control the bias and precharge transistors of the respective page buffers to fix  
the first sense nodes at the predetermined bias voltage during a second sensing period when  
voltages on the second sense nodes are being sensed.

20      3. A non-volatile memory device according to claim 1, wherein, during the first  
sensing period, the first sense nodes are configured to be connected to or floated from  
corresponding columns based on a state of respective memory cells of the corresponding  
columns, and wherein the second sense nodes are configured to be fixed at the predetermined  
25      bias voltage.

4        4. A non-volatile memory device according to claim 3, wherein, during the  
second sensing period, the second sense nodes are configured to be connected to or floated  
from corresponding columns based on a state of respective memory cells of the  
30      corresponding columns, and wherein the first sense nodes are configured to be fixed at the  
predetermined bias voltage.

5. A non-volatile memory device according to claim 4, wherein each of the  
columns comprises two bit lines.

6. A non-volatile memory device according to claim 5, wherein a first one of the bit lines of each column is configured to be selected during the first or second sensing period, and wherein a second one of the bit lines is configured not to be selected during the first and second sensing periods.

7. A non-volatile memory device according to claim 3, wherein even-numbered ones of the first bit lines of the columns are configured to be selected during the first sensing period and wherein odd-numbered ones of the first bit lines are configured to be selected during the second sensing period.

8. A non-volatile memory device according to claim 7, wherein the predetermined voltage is either a power supply voltage or a ground voltage.

15 9. A flash electrically erasable and programmable read-only memory (EEPROM) device comprising:

a memory cell array comprising a plurality of cell strings, wherein each of the cell strings comprises a plurality of memory cells arranged in series between a first string select transistor and a second string select transistor;

20 a plurality of bit lines connected to the strings, wherein the bit lines are divided into a plurality of bit line groups, each group comprising two bit lines;

a plurality of page buffers, wherein each page buffer corresponds to one of the bit line groups, and wherein each of the page buffers comprises a bit line select section configured to select one of the bit lines of each bit line group, a precharge section configured to supply a

25 variable current to a sense node connected to a corresponding bit line group through a bit line bias section, a latch section configured to latch data determined according to a voltage of the sense node, and a switch section connected between the sense node and the latch section; and

30 a page buffer control logic configured to control the precharge section of each page buffer such that during a first sensing period, when data is read out from memory cells in a selected page through first ones of the bit lines of first bit line groups, sense nodes corresponding to second bit line groups are fixed at a predetermined bias voltage.

10. A flash EEPROM device according to claim 9, wherein the page buffer control logic is further configured to control the precharge section of each page buffer such

that sense nodes corresponding to first bit line groups are fixed at the predetermined bias voltage during a second sensing period when data is read out from memory cells in the selected page through first ones of bit lines of the second bit line groups.

5        11. A flash EEPROM device according to claim 10, wherein the bias voltage is either a power supply voltage or a ground voltage.

12. A non-volatile semiconductor memory device comprising:  
an array of memory cells arranged in a plurality of rows and columns;

10        a plurality of page buffers each connected to the columns, wherein each of the page buffers comprises a bias transistor connected between a corresponding column and a corresponding sense node, a latch connected to the corresponding sense node, a precharge transistor connected between a power supply voltage and the corresponding sense node, and a switch transistor connected between the latch and the corresponding sense node; and

15        a control logic configured to control the page buffers during a read operation, wherein the control logic is configured to control the bias transistor, the precharge transistor, and the switch transistor of the page buffers such that second sense nodes are fixed at a predetermined bias voltage during a first sense period when voltages on first sense nodes are sensed.

20        13. A flash EEPROM device according to claim 12, wherein the control logic is further configured to control the bias, precharge, and switch transistors of each of the page buffers such that first sense nodes are fixed at the bias voltage during a second sense period when voltages on second sense nodes are sensed.

25        14. A non-volatile memory device according to claim 12, wherein during the first sensing period, the first sense nodes are configured to be connected to or floated from corresponding columns based on a state of respective memory cells, and wherein the second sense nodes are configured to be fixed at the predetermined voltage.

30        15. A non-volatile memory device according to claim 13, wherein, during the second sensing period, each of the second sense nodes is configured to be connected to or floated from a corresponding column based on a state of a respective memory cell, and wherein the first sense nodes are configured to be fixed at the predetermined voltage.

16. A flash EEPROM device according to claim 15, wherein the bias voltage is either a power supply voltage or a ground voltage.

5        17. A non-volatile memory device comprising:  
          a memory cell array having a plurality of strings, each string comprising a plurality of memory cells connected in series between a first select transistor and a second select transistor;  
          a plurality of bit lines each connected to the strings, wherein the bit lines are divided  
10 into a plurality of bit line groups, each bit line group comprising a plurality of bit lines;  
          a plurality of page buffers corresponding to the bit line groups, wherein each of the page buffers comprises a bit line select section for selecting a bit line of each bit line group, a precharge section for supplying a variable current to a sense node connected to a corresponding bit line group through a bit line bias section, a latch section for latching data  
15 determined according to a voltage of the sense node, and a switch section connected between the sense node and the latch section; and  
          a page buffer control logic configured to control the precharge and switch sections of each page buffer such that during a first sensing period, when data is read out from memory cells in a selected page through first ones of bit lines of first bit line groups, sense nodes  
20 corresponding to second bit line groups are fixed at a predetermined bias voltage.

18. A flash EEPROM device according to claim 17, wherein the page buffer control logic is configured to control the precharge and switch sections of each page buffer such that sense nodes corresponding to first bit line groups are fixed at the predetermined bias  
25 voltage during a second sensing period when data is read out from memory cells in the selected page through first ones of bit lines of the second bit line groups.